

P-Ch 100V Fast Switching MOSFETs

- ★ Super Low Gate Charge
- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

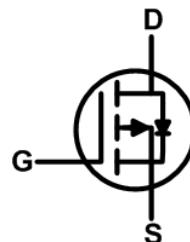
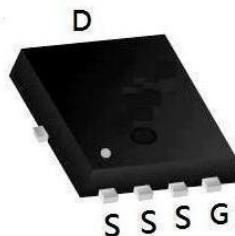

Product Summary

BVDSS	RDS(ON)	ID
-100V	70mΩ	-25A

Description

The XXW20P10F is the high cell density trenched P-ch MOSFETs, which provide excellent RDS(ON) and gate charge for most of the synchronous buck converter applications.

The XXW20P10F meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

PDFN5060-8L Pin Configuration

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	-20	A
		-11	
Pulsed Drain Current ¹	I_{DM}	-72	A
Single Pulse Avalanche Energy ²	E_{AS}	42	mJ
Total Power Dissipation	P_D	102	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient ³	$R_{\theta JA}$	91	°C/W
Thermal Resistance from Junction-to-Case	$R_{\theta JC}$	1.22	°C/W

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Electrical Characteristics ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0V, I_D = -250\mu\text{A}$	-100	-	-	V
Gate-body Leakage current	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	± 100	nA
Zero Gate Voltage Drain Current $T_J = 25^\circ\text{C}$ $T_J = 100^\circ\text{C}$	I_{DSS}	$V_{DS} = -100V, V_{GS} = 0V$	-	-	-1	μA
			-	-	-20	
Gate-Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-1.5	-2	-2.5	V
Drain-Source On-Resistance ⁴	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -10\text{A}$	-	70	88	$\text{m}\Omega$
		$V_{GS} = -4.5V, I_D = -6\text{A}$		77	97	
Forward Transconductance ⁴	g_f	$V_{DS} = -10V, I_D = -10\text{A}$	-	28	-	S
Dynamic Characteristics⁵						
Input Capacitance	C_{iss}	$V_{DS} = -50V, V_{GS} = 0V, f = 1\text{MHz}$	-	2859	-	pF
Output Capacitance	C_{oss}		-	93	-	
Reverse Transfer Capacitance	C_{rss}		-	68	-	
Gate Resistance	R_g	$f = 1\text{MHz}$	-	4.3	-	Ω
Switching Characteristics⁵						
Total Gate Charge	Q_g	$V_{GS} = -10V, V_{DS} = -50V, I_D = -10\text{A}$	-	53	-	nC
Gate-Source Charge	Q_{gs}		-	12	-	
Gate-Drain Charge	Q_{gd}		-	10	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -10V, V_{DD} = -50V, R_G = 3\Omega, I_D = -10\text{A}$	-	8	-	ns
Rise Time	t_r		-	27	-	
Turn-Off Delay Time	$t_{d(off)}$		-	155	-	
Fall Time	t_f		-	77	-	
Body Diode Reverse Recovery Time	t_{rr}		-	36	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}	$I_F = -10\text{A}, dI/dt = 100\text{A}/\mu\text{s}$	-	40	-	nC
Drain-Source Body Diode Characteristics						
Diode Forward Voltage ⁴	V_{SD}	$I_S = -10\text{A}, V_{GS} = 0V$	-	-0.9	-1.3	V
Continuous Source Current	I_S	-	-	-	20	A

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(\text{MAX})}=150^\circ\text{C}$.
2. The EAS data shows Max. rating . The test condition is $V_{DD} = -35V, V_{GS} = -10V, L = 0.5\text{mH}, I_{AS} = -23\text{A}$
3. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
5. This value is guaranteed by design hence it is not included in the production test..

Typical Performance Characteristics

Fig 1: Output Characteristics

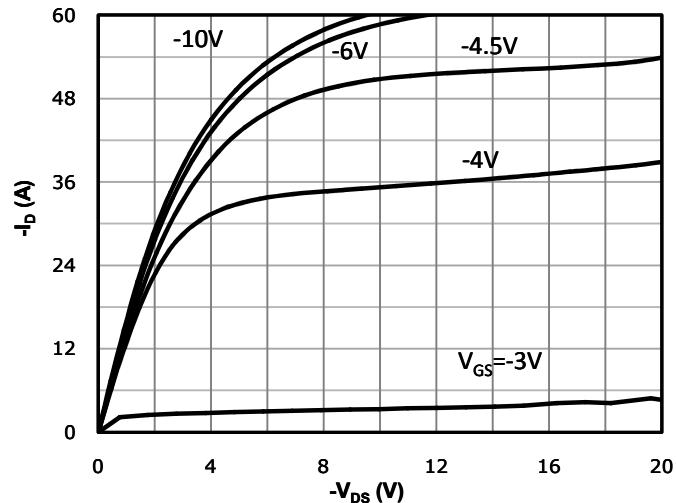


Fig 2: Transfer Characteristics

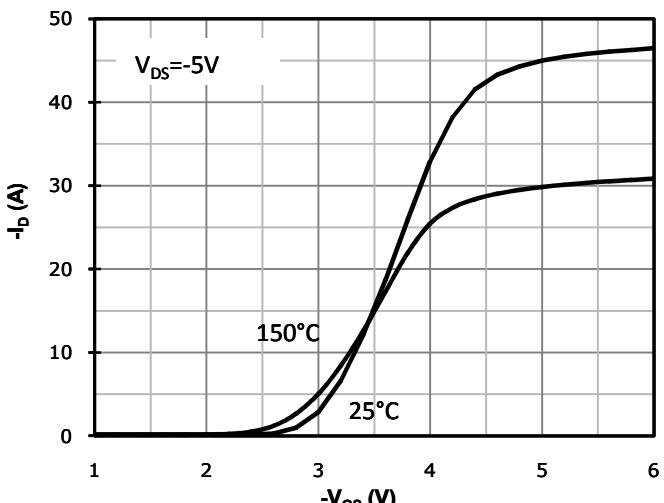


Fig 3: $R_{DS(on)}$ vs Drain Current and Gate Voltage

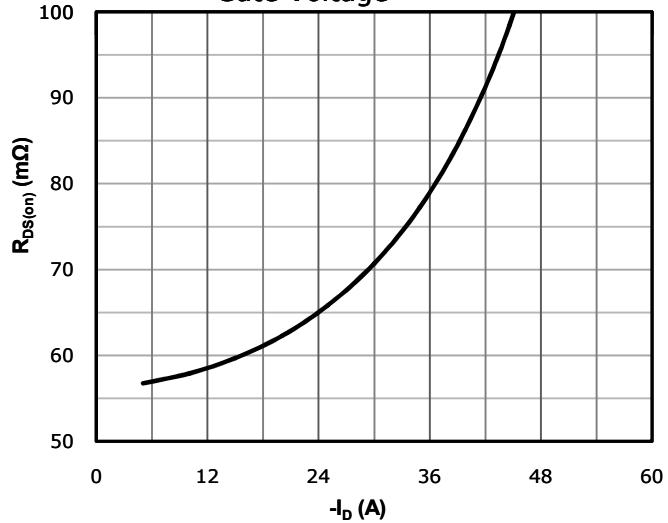


Fig 4: $R_{DS(on)}$ vs Gate Voltage

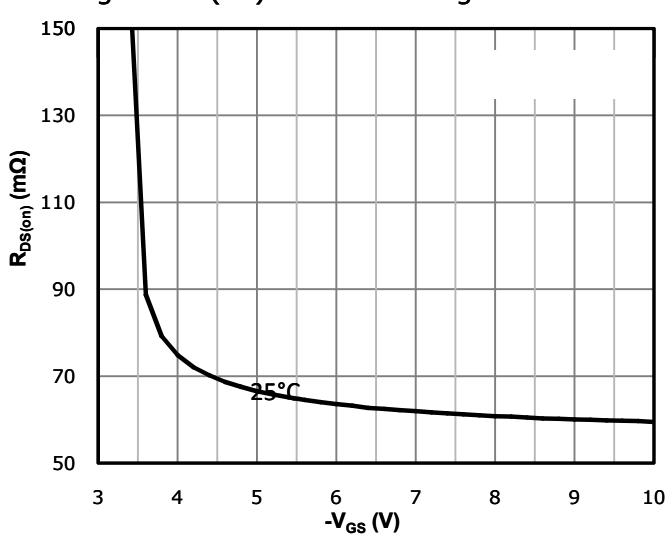


Fig 5: $R_{DS(on)}$ vs. Temperature

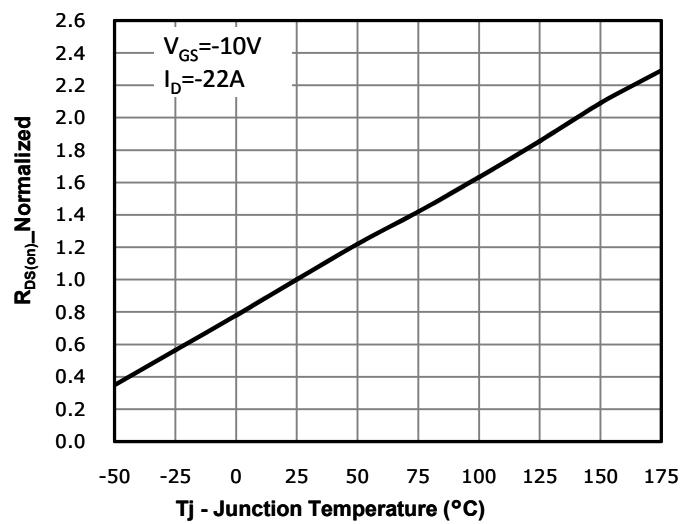
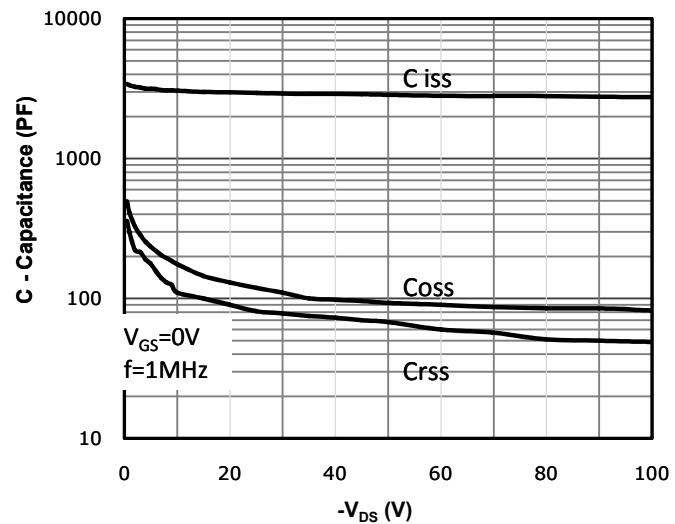


Fig 6: Capacitance Characteristics



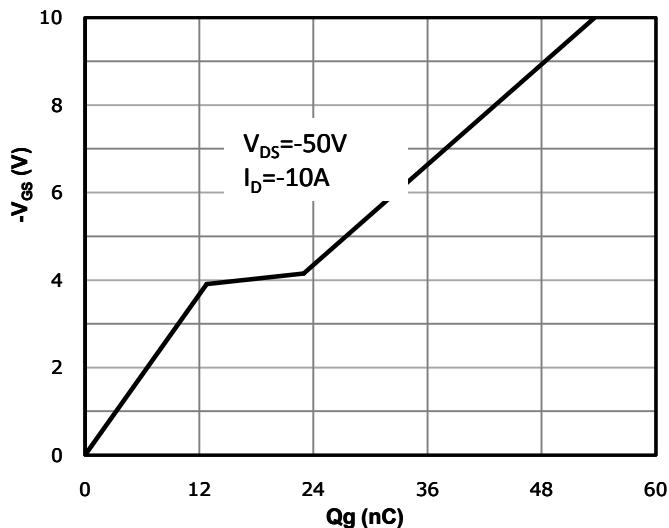
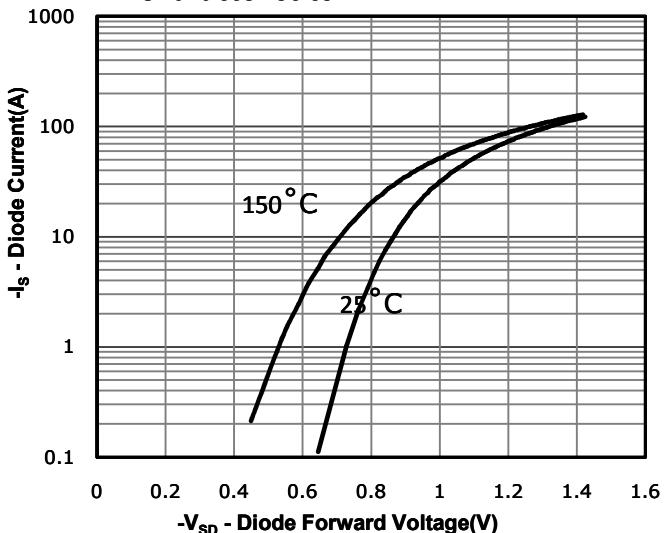
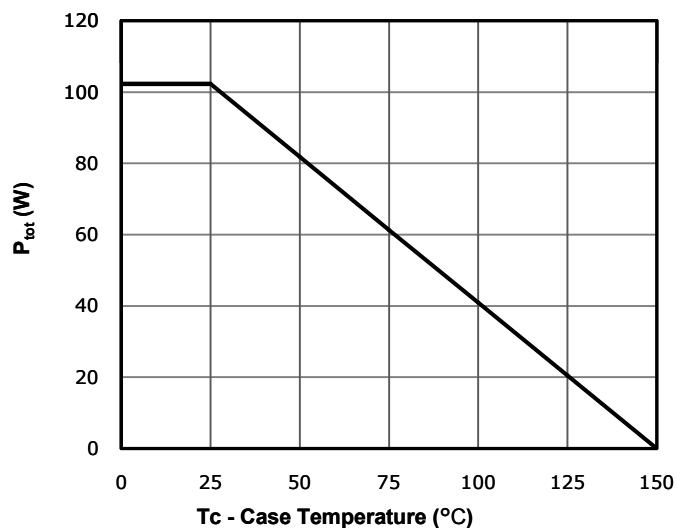
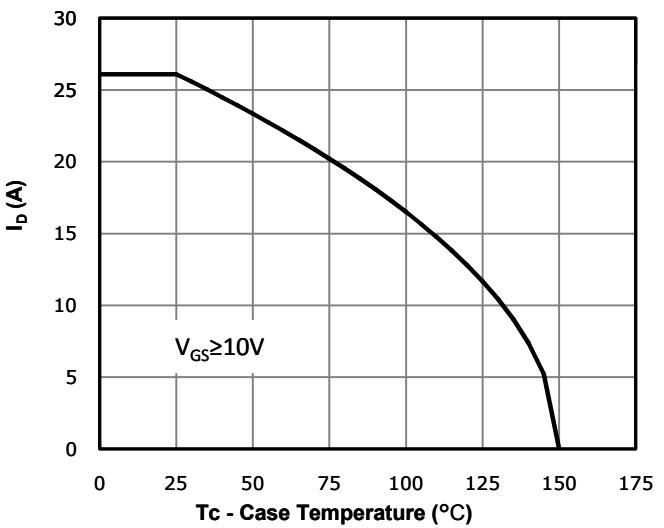
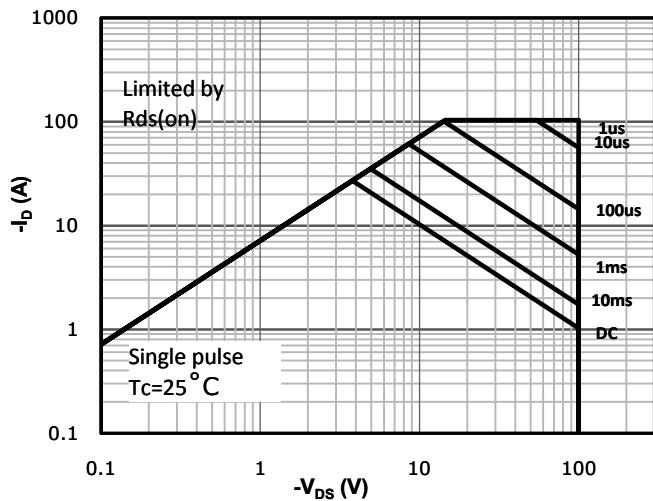
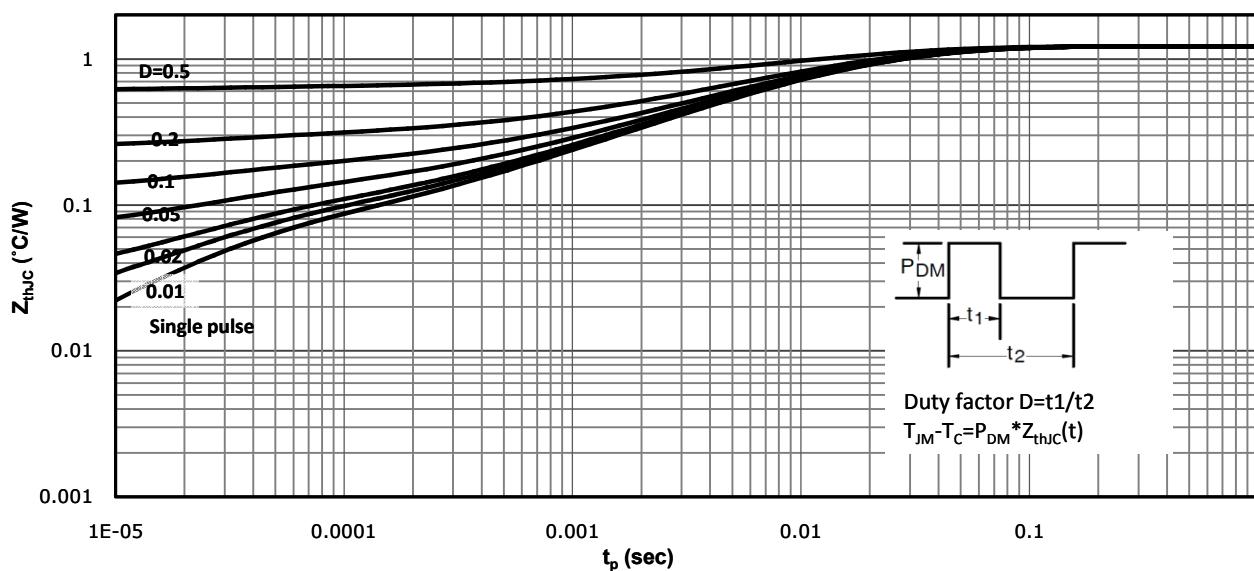
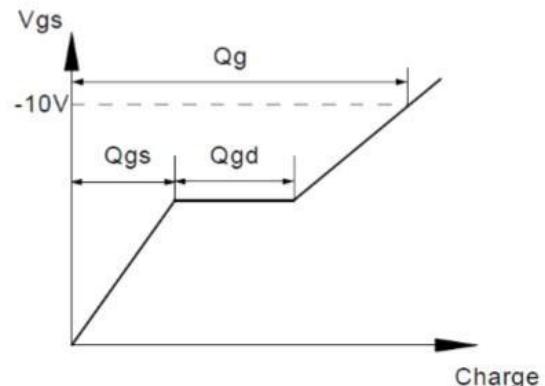
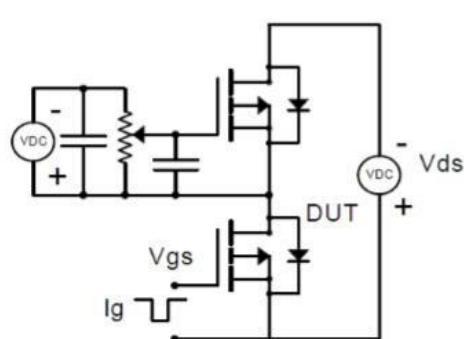
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Fig 7: Gate Charge Characteristics

Fig 8: Body-diode Forward Characteristics

Fig 9: Power Dissipation

Fig 10: Drain Current Derating

Fig 11: Safe Operating Area


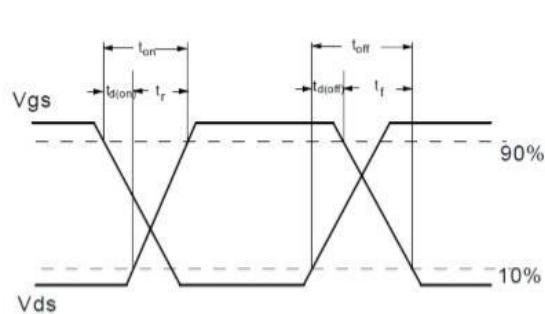
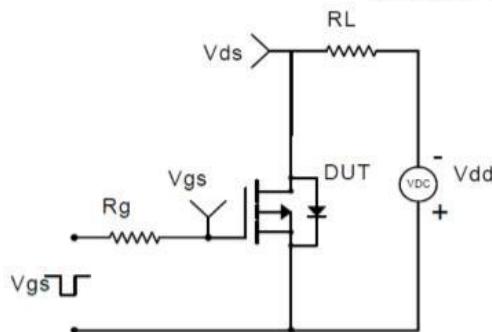
Fig 12: Max. Transient Thermal Impedance


Test Circuit & Waveform

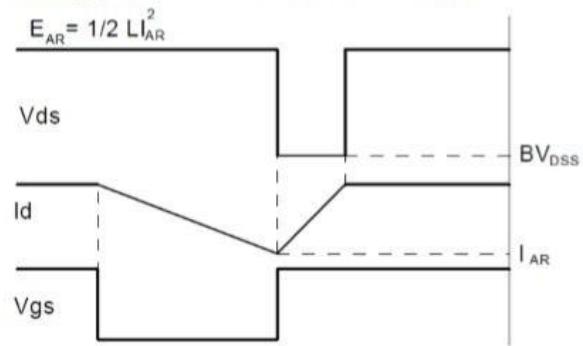
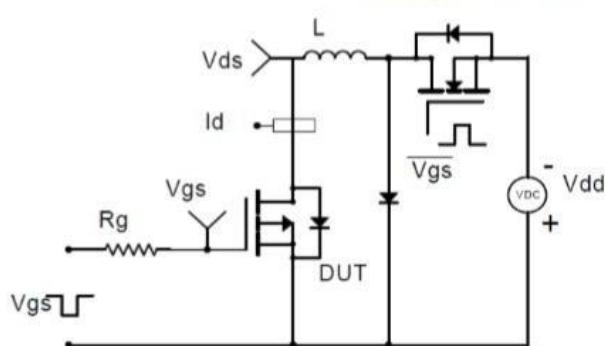
Gate Charge Test Circuit & Waveform



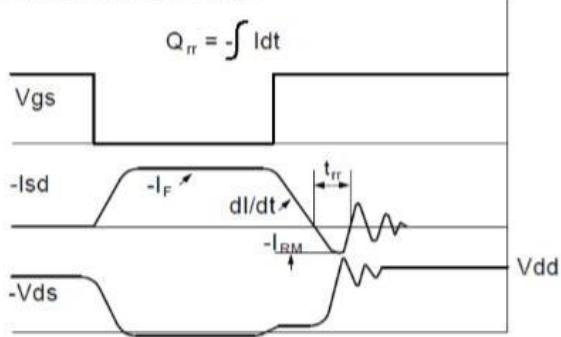
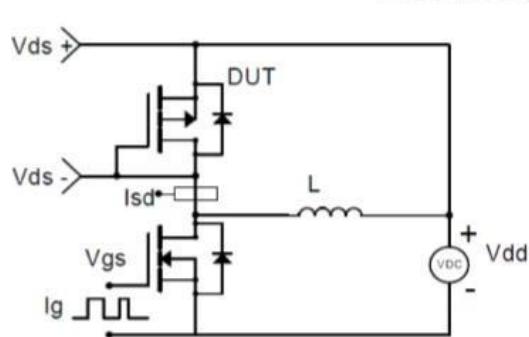
Resistive Switching Test Circuit & Waveforms

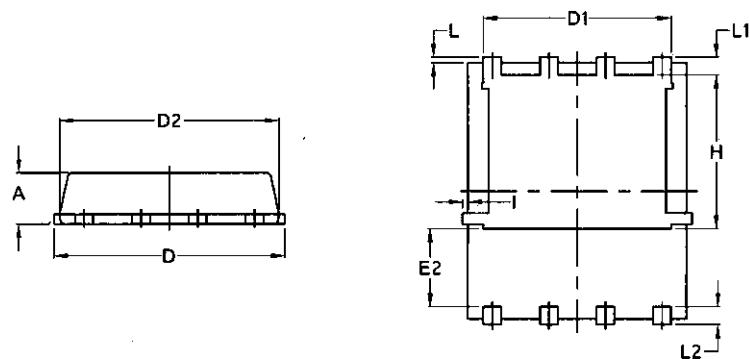
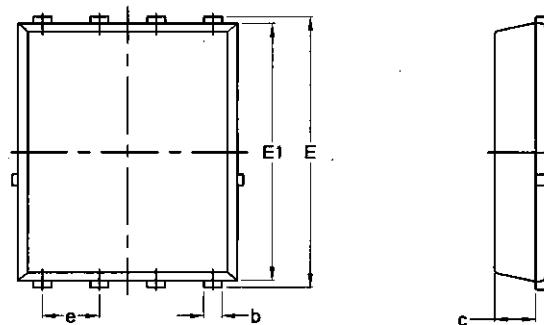


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Mechanical Data-PDFN5060-8L-Single


Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070