

- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology



Product Summary

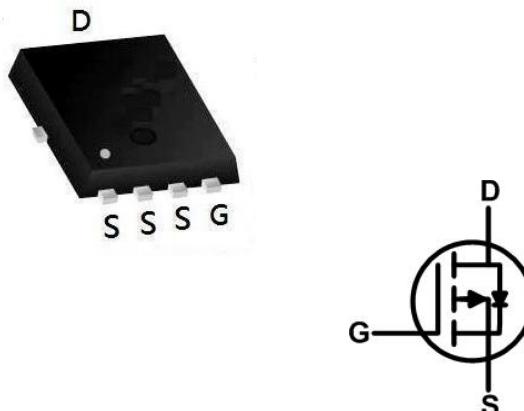
BVDSS	RDS(ON)	ID
-40V	10mΩ	-40A

Description

The XXW40P04F is the high cell density trenched P-ch MOSFETs, which provide excellent RDS(ON) and gate charge for most of the synchronous buck converter applications.

The XXW40P04F meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

PDFN5060-8L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-40	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_c = 25^\circ C$	Continuous Drain Current, $-V_{GS} @ -10V^1$	-40	A
$I_D @ T_c = 100^\circ C$	Continuous Drain Current, $-V_{GS} @ -10V^1$	-25	A
I_{DM}	Pulsed Drain Current ²	-160	A
EAS	Single Pulse Avalanche Energy ³	144	mJ
I_{AS}	Avalanche Current	-30.0	A
$P_D @ T_c = 25^\circ C$	Total Power Dissipation ⁴	45	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	62	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	3.6	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D = -250\mu\text{A}$	-40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -40\text{V}$, $V_{GS}=0\text{V}$	-	-	-1	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS}=0\text{V}$, $V_{GS}= \pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D = -250\mu\text{A}$	-1.0	-1.7	-2.5	V
$R_{DS(\text{on})}$ note3	Static Drain-Source on-Resistance	$V_{GS} = -10\text{V}$, $I_D = -20\text{A}$	-	10	13	$\text{m}\Omega$
		$V_{GS} = -4.5\text{V}$, $I_D = -10\text{A}$	-	14	17	
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = -20\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	3800	-	pF
C_{oss}	Output Capacitance		-	329	-	pF
C_{rss}	Reverse Transfer Capacitance		-	289	-	pF
Q_g	Total Gate Charge	$V_{DS} = -20\text{V}$, $I_D = -20\text{A}$, $V_{GS} = -10\text{V}$	-	68	-	nC
Q_{gs}	Gate-Source Charge		-	10	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	14	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = -20\text{V}$, $I_D = -20\text{A}$, $V_{GS} = -10\text{V}$, $R_{GEN}=2.4\Omega$	-	10	-	ns
t_r	Turn-on Rise Time		-	82	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	93	-	ns
t_f	Turn-off Fall Time		-	74	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	-40	-	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	-160	-	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}$, $I_S = -30\text{A}$	-	-0.8	-1.2	V
trr	Reverse Recovery Time	$V_{GS}=0\text{V}$, $I_S = -30\text{A}$, $di/dt=100\text{A}/\mu\text{s}$	-	20	-	ns
Qrr	Reverse Recovery Charge		-	13	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: $T_J= 25^\circ\text{C}$, $V_{DD}= -20\text{V}$, $V_G= -10\text{V}$, $L= 0.5\text{mH}$, $R_G= 25\Omega$, $I_{AS}= -24\text{A}$

3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

Typical Performance Characteristics

Figure1: Output Characteristics

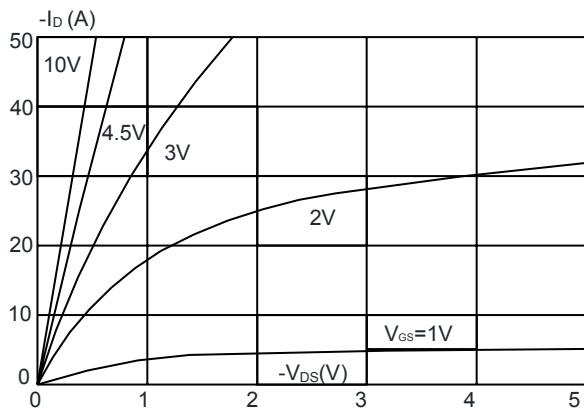


Figure 3: On-resistance vs. Drain Current

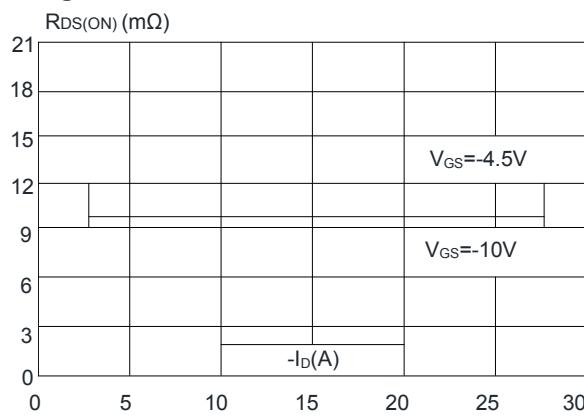


Figure 5: Gate Charge Characteristics

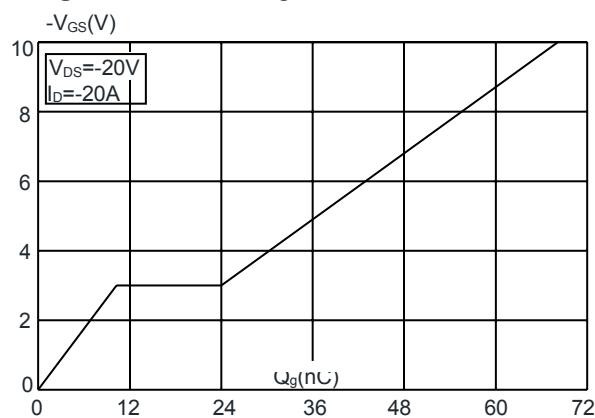


Figure 2: Typical Transfer Characteristics

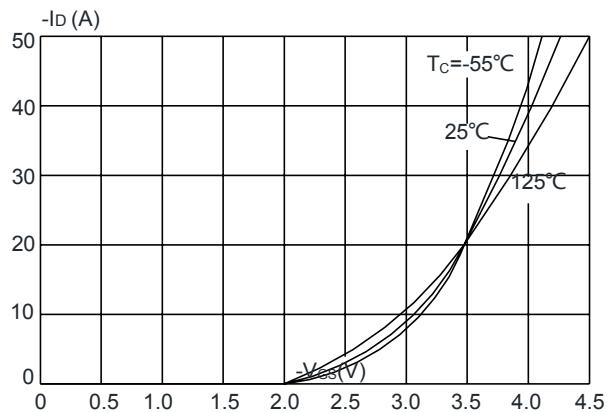


Figure 4: Body Diode Characteristics

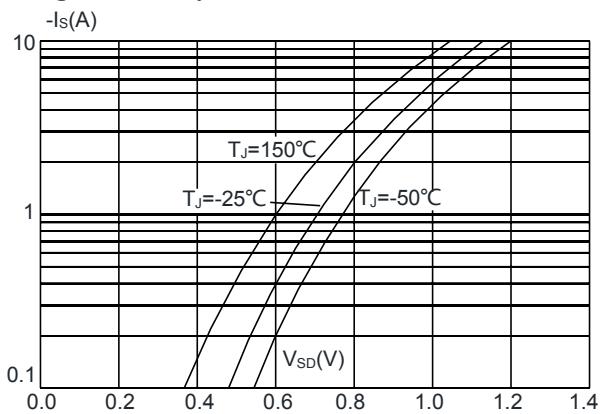


Figure 6: Capacitance Characteristics

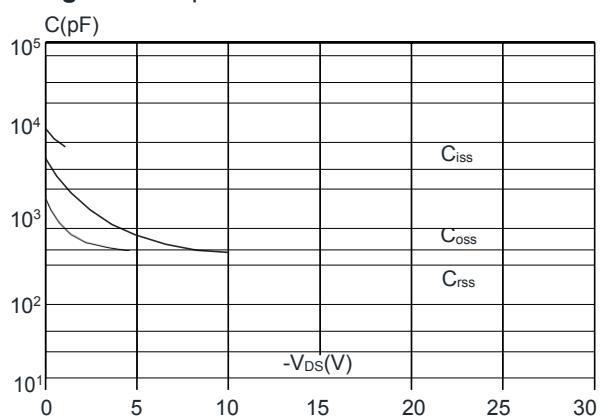


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

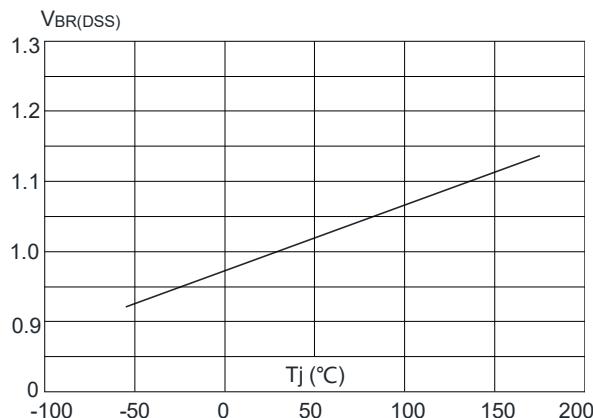


Figure 8: Normalized on Resistance vs. Junction Temperature

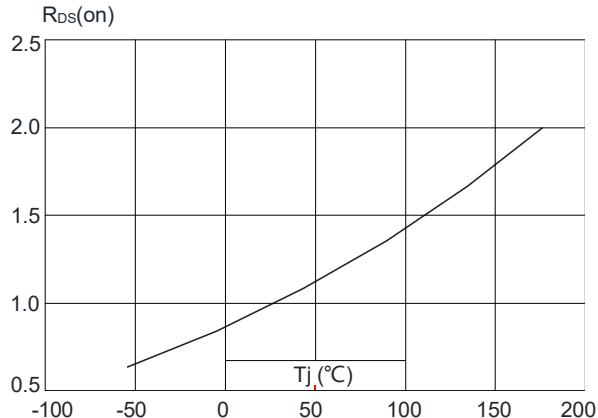


Figure 9: Maximum Safe Operating Area

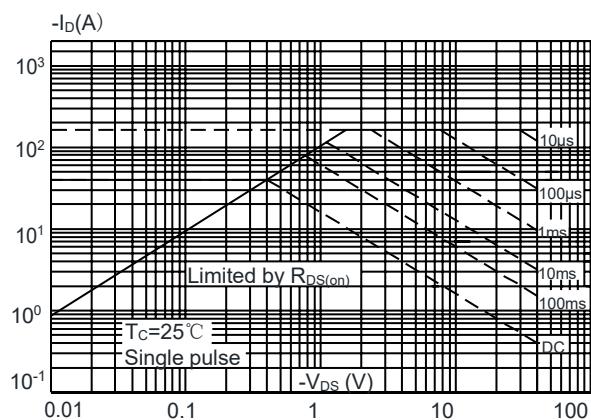


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

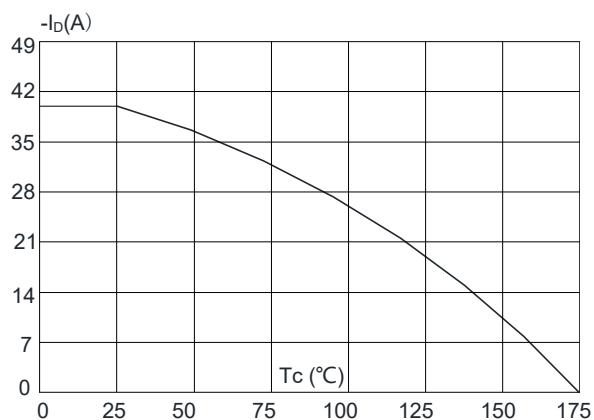
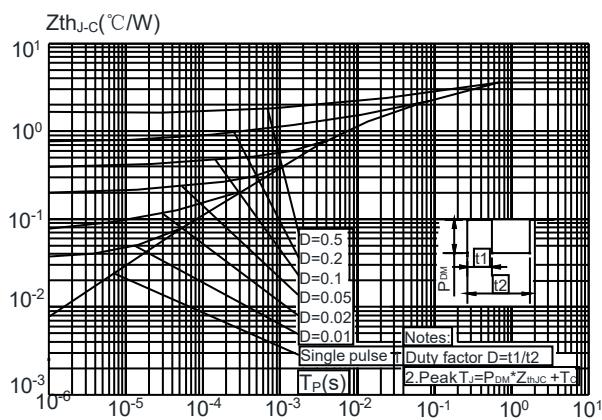
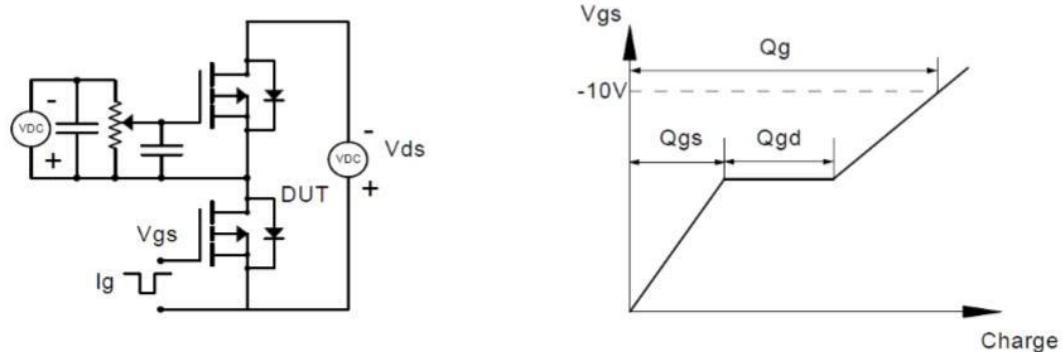


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

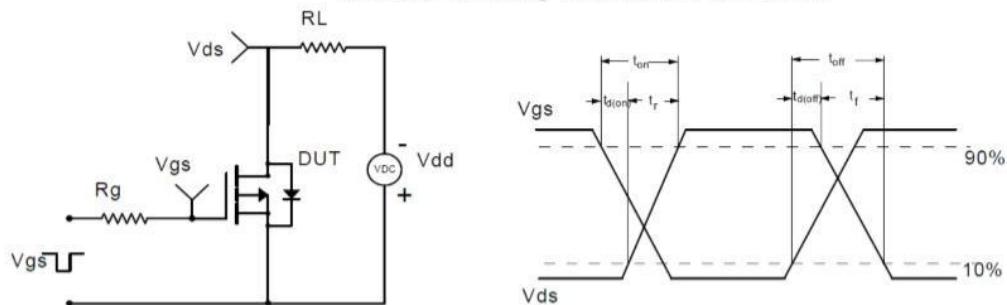


Test Circuit

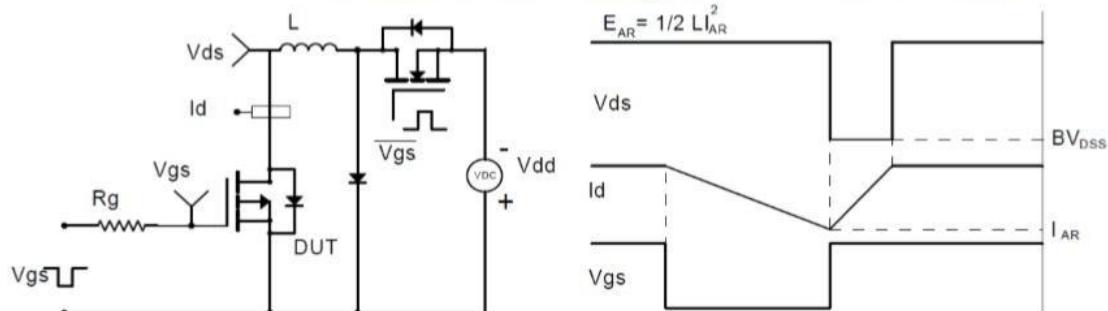
Gate Charge Test Circuit & Waveform



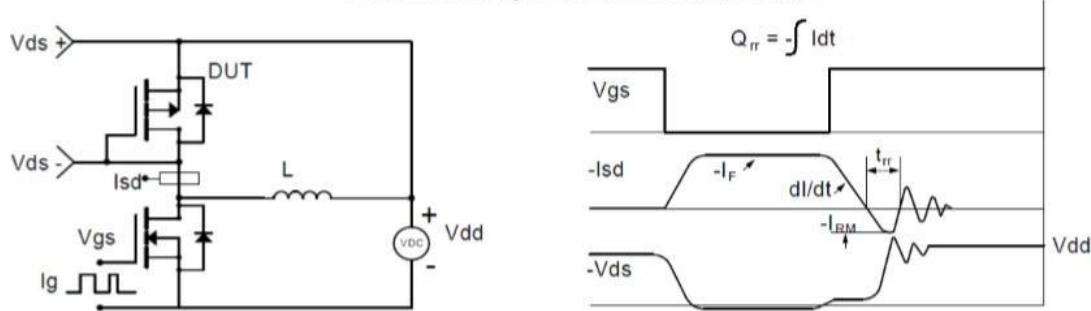
Resistive Switching Test Circuit & Waveforms

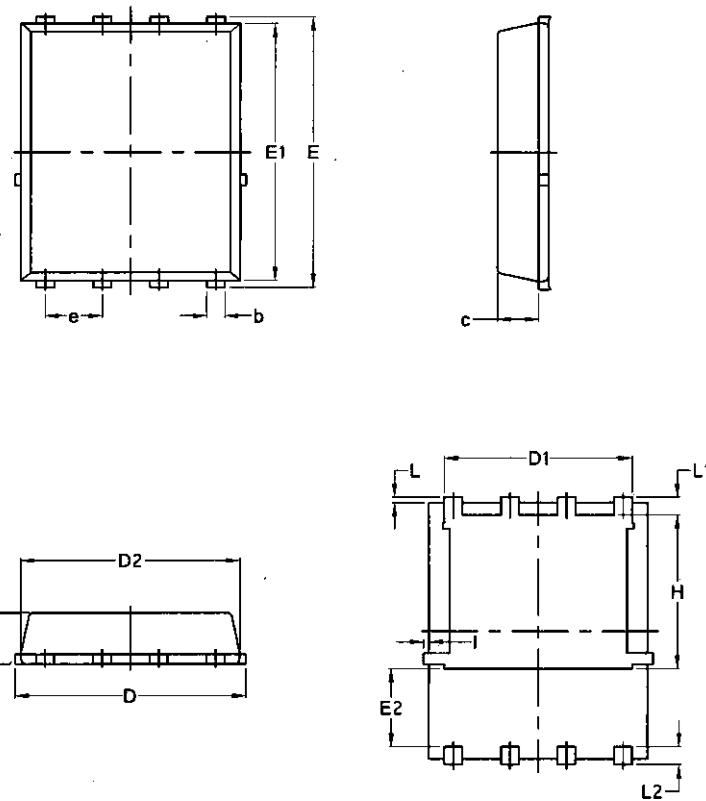


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Mechanical Data-PDFN5060-8L-Single


Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070